A 60GHz - BAND ULTRA LOW NOISE PLANER - DOPED HEMT

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ABSTRACT

An ultra low noise AlGaAs/InGaAs HEMT with a 0.15μm T-shaped gate and Si planer-doped layer has been developed for millimeter-wave systems. The HEMT showed the extremely reduced minimum noise figure of 1.6dB and high associated gain of 6.5dB at 60GHz. The noise figure is the lowest value ever reported for the AlGaAs/InGaAs pseudomorphic HEMT.

INTRODUCTION

Recent developments in heterostructure transistor technology have advanced very rapidly outstanding low-noise amplification results throughout the microwave and millimeter-wave frequency range [1-3]. Applications requiring low-noise, high-gain performance such as radar, communication, remote sensing, electronics warfare find HEMTs crucial to realize the requirements.

The HEMTs must be designed in consideration of the high trans-conductance (g_m), the low parasitics, and the precise measurement for realization of the high performance for millimeter-wave.

In this paper, we report the development of an ultra low noise AlGaAs/InGaAs pseudomorphic HEMT with a 0.15μm T-shaped gate, and discuss a way to improve the accuracy of millimeter-wave measurement.

PROCESS

Figure 1 shows schematic a cross-section of the HEMT. The HEMT layers consist of ; (i) 200Å InGaAs channel (ii) 30Å Si-doped n-AlGaAs layer with density of $2x10^{18}cm^{-3}$ (iii) Si-planer doped layer with sheet carrier concentrations of $5x10^{12}cm^{-2}$ (vi) 200Å n-AlGaAs layer (v) 1000Å n-GaAs cap layer. In order to reduce Rs, the undoped spacer layer was not formed. These epitaxial layers were grown by molecular beam epitaxy on a 3-inch semi-

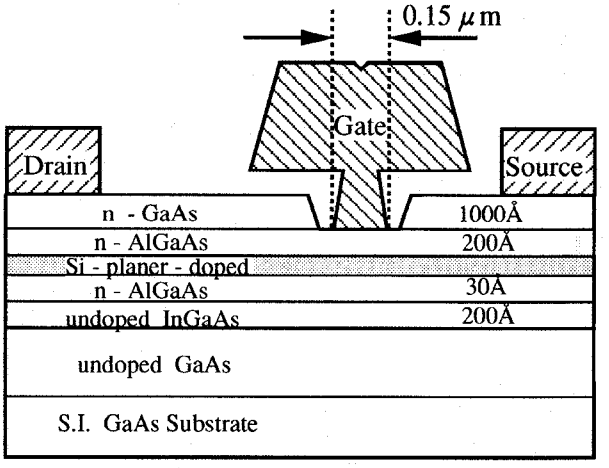

Fig.1 Schematic cross-sections of the planer-doped HEMT

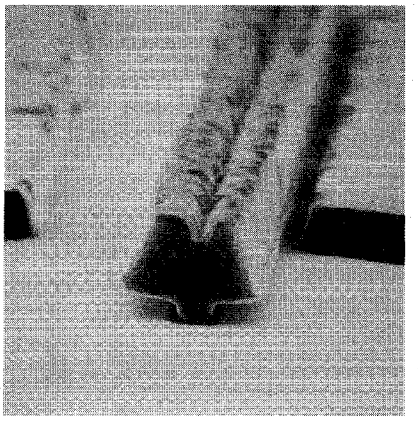

Fig.2 Cross sectional SEM micrograph of the 0.15 μm T-shaped gate

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insulating GaAs substrate. Ohmic contacts were formed by alloying the EB-evaporated Au/Ni/AuGe defined by a conventional lifting-off process. The spacing between source and drain electrodes is 1.5μm. The device isolation was performed using H^+ implantation.

In delineating the T-shaped gate electrode, a double layer resist process has been adopted[4]. The gate length was 0.15μm. Figure 2 shows the cross sectional SEM micrograph of the T-shaped gate. The device was passivated with an SiON film.

CHARACTERISTICS

Figure 3 shows the microphotograph of the HEMT. Maximum g_m is as high as 680mS/mm. It is improved more than 30% compared to the conventional HEMT's (by planer-doping).

S-parameters of the HEMT was measured by an on-wafer-probing method up to 60GHz. And the effect of parasitics, which include the capacitance of the bonding pads, was corrected in the Y-parameter domain [5]. Figure 4 shows the process of the correction.

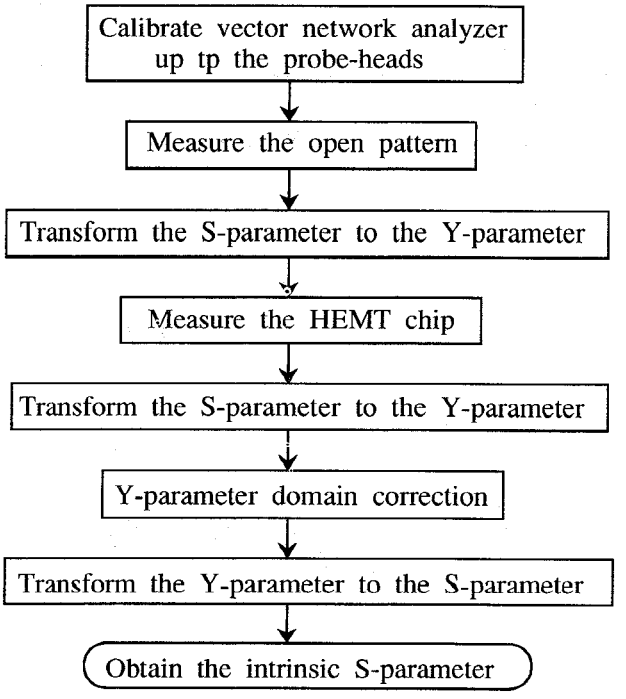


Fig. 4 Process of the correction of Y-parameter domain

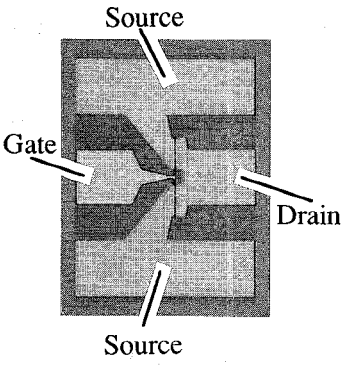


Fig.3 Microphotograph of the HEMT ($W_g = 100\ \mu m$)

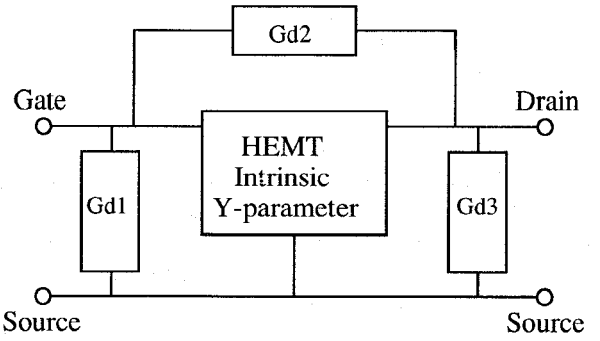


Fig.5 Equivalent parasitic admittance circuit of measured HEMT

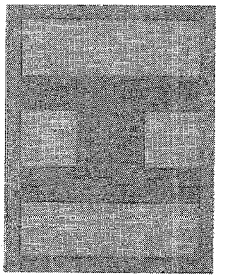


FIg.6 Microphotograph of the open pattern

Figure 5 shows an equivalent parasitic admittance circuit, which is in parallel of the HEMT. The parasitic admittance (Gd1,Gd2,Gd3) can be canceled by using measured Y-parameters of the HEMT and the open-pattern. Figure 6 shows the open-pattern (dummy) used in the correction. This pattern consists of bonding pads, without the transistor. As a result, we can cancel the parasitic capacitance rated to the bonding pads, and obtain the intrinsic S-parameters.

In figure 7, |H21| obtained from "measured S-parameter" and "corrected S-parameter" are plotted against frequency. After the Y-parameter correction, the cut-off frequency (f_T) was improved up to 78GHz from 66GHz. The maximum frequency of oscillation (f_{max}) was estimated to be 180GHz from the intrinsic S-parameter.

Figure 8 shows the equivalent circuit and the elemental parameters extracted from the measured and corrected data. After the correction, the gate-pad capacitance (C_{pg}) and the drain-pad capacitance (C_{pd}) were reduced to approximately 60% compare to the measured value. The additional capacitance, which is considered mainly the gate/drain electrode fringing capacitance, occupies 60% of the total C_{pg} or C_{pd}. Meanwhile, the gate inductance (L_g) and the drain inductance (L_d) as series parasitics, were hardly canceled by this correction.

The Y-parameter correction is effective especially in case of designing MMICs because we can reduce the influence of the bonding pads easily and selectively.

To improve the accuracy of noise figure measurement, the second stage noise should be reduced. So, we use the following configuration.

A passive circuit chip which includes the matching and the bias circuits were fabricated. The chip showed the small insertion loss of 0.4dB and the low VSWR of 1.2 at 60GHz. Figure 9 shows measured insertion loss and VSWR of the passive circuit chip.

Then, the HEMT chip was mounted between the input and the output circuits chips laid on a metal carrier. Figure 10 shows the microphotograph of the assembled chips. This configuration does not demand the tuners for impedance matching, the attenuators to prevent undesirable low frequency oscillation, and the bias-tees out of the jig. Because of the removal of these system elements, the second-stage-noise in this configuration was reduced to about 5dB, and was smaller than the conventional configuration by 4dB or above. As a result, the accuracy of noise figure was expected to be less

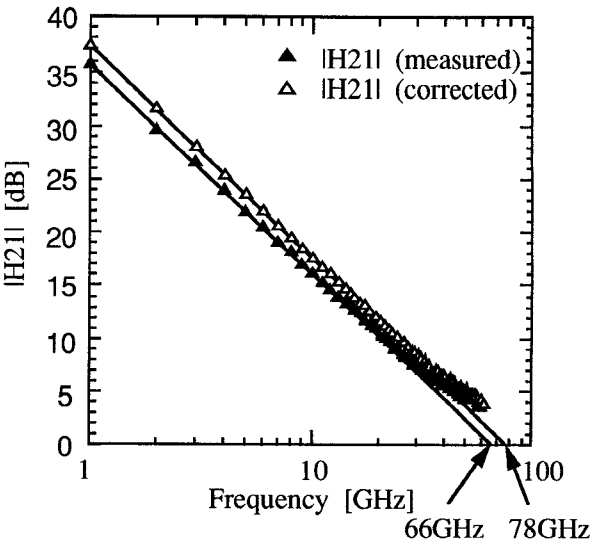
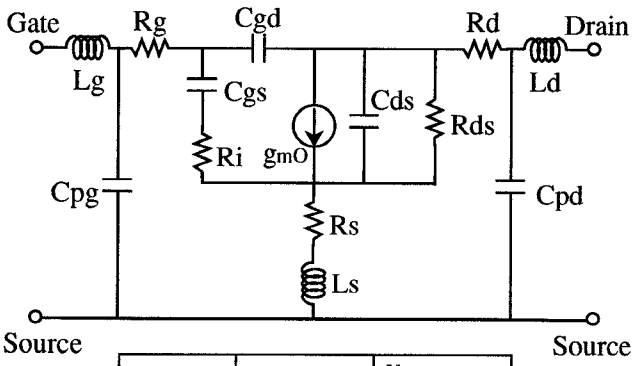


Fig.7 Measured and Y-parameter corrected |H21| versus frequency



	Measured	Y- parameter corrected
Lg [pH]	64	62
Ls [pH]	9	10
Ld [pH]	14	9
Rg [Ω]	1.2	←
Rs [Ω]	3.8	←
Rd [Ω]	7.4	←
Cpg [fF]	33	20
Cpd [fF]	35	21
Cgs [fF]	58	←
Cgd [fF]	15	←
Cds [fF]	3	←
Ri [Ω]	8.2	←
Rds [Ω]	260	←
gmo [mS]	55	←

Fig.8 Equivalent circuit of the HEMT and its element values (Wg/Lg = 80 μm/0.15 μm)

than ±0.15dB.

The most lowest minimum noise figure (Fmin) of 1.6dB with associated gain (Ga) of 6.5dB has been obtained at 60GHz for a 100μm gate-width HEMT. Figure 11 shows a Fmin and Ga versus Ids plot.

CONCLUSION

An ultra low noise AlGaAs/InGaAs HEMT with 0.15μm T-shaped gate has been developed. The HEMT showed high g_m of 680mS/mm caused by planer-doping, Fmin of as low as 1.6dB, and high Ga of 6.5dB. The value of Fmin is one of the lowest value ever reported for the AlGaAs/InGaAs pseudomorphic HEMT. The HEMT in this work is practical enough for the millimeter-wave radar or communication systems.

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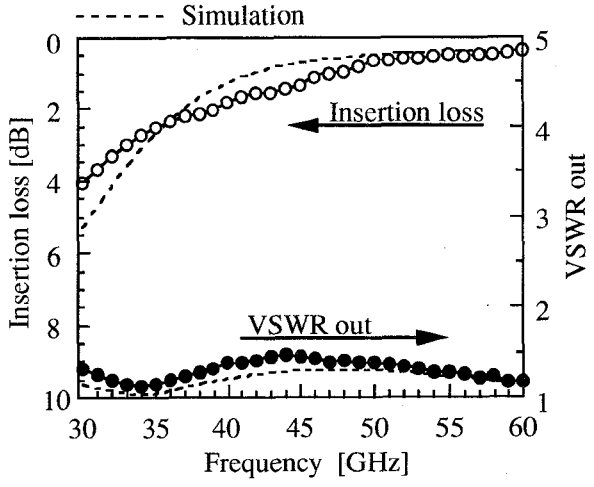

Fig.9 Insertion loss and VSWR of the passive circuit chip

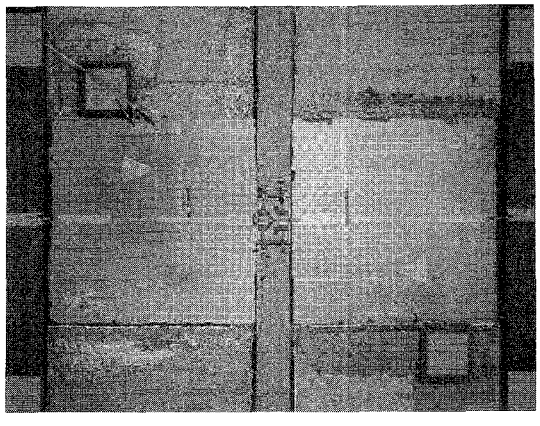

Fig.10 Microphotograph of the matching/bias circuit chip (2mmx2mm)

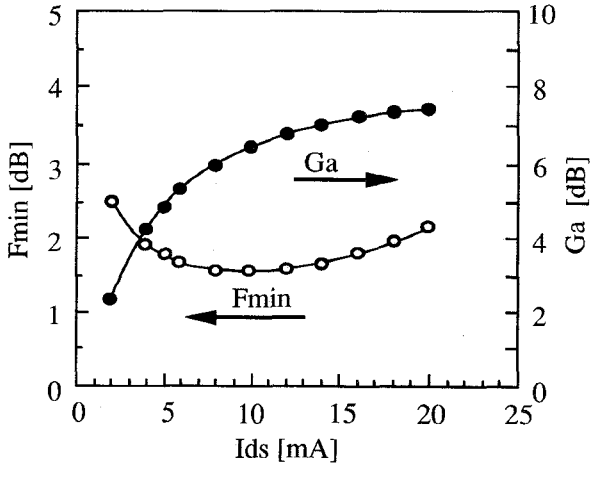

Fig.11 Ids dependence of Fmin and Ga (f=60GHz)